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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/508,915	04/21/2005	Hiroshi Miyagi	TIC-0073	8214

23377 7590 09/25/2006

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EXAMINER	
WENDELL, ANDREW	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/508,915	MIYAGI, HIROSHI	
	Examiner	Art Unit	
	Andrew Wendell	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *06 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Myer (US Pat# 5,012,490) in view of Lee et al. (US Pat# 5,774,555).

Regarding claim 1, Myer's varying bandwidth digital signal detector teaches a receiver which converts a received signal directly to a baseband signal (Col. 4 lines 55-62), comprising a switched-capacitor filter 405 (Fig. 4, Col. 5 lines 57-58) controlling a cutoff frequency when the baseband signal RBS (Fig. 4) is filtered according to a control signal FBC (Fig. 4) provided for a switched-capacitor element; an oscillator generating a periodic signal 425 (Fig. 4); and a periodic signal generated by the oscillator 425 (Fig. 4) according to the received signal, an output signal from the control signal FBC (Fig. 4) for the switched-capacitor element 405 (Fig. 4, Col. 4 line 55-Col. 5 line 58). Myer fails to teach a phase locked loop having a first and second divider used for a control signal.

Lee et al. switched capacitor bandpass filter teaches a receiver, comprising a switched-capacitor filter 334 (Fig. 5) controlling a cutoff frequency when the signal is filtered according to a control signal 1/M (Fig. 5) provided for a switched-capacitor element 334 (Fig.5); an oscillator 326 (Fig. 5) generating a periodic signal; a phase

locked loop circuit 320 (Fig. 5) comprising a first divider 1/N (Fig. 5), wherein the PLL circuit generates a periodic signal of a predetermined frequency according to an output signal from the first divider 1/N (Fig. 5) and the periodic signal generated by the oscillator 326 (Fig. 5); and a second divider 1/M (Fig. 5) further dividing the periodic signal generated by the PLL circuit 320 (Fig. 5) according to the received signal, wherein the output signal from the second divider 1/M (Fig. 5) is provided as the control signal for the switched-capacitor element 334 (Fig. 5 and Col. 5 line 36-Col. 6 line 6).

Therefore, at the time the invention was made it would have been obvious to one skilled in the art to incorporate a divider used for a control signal as taught by Lee et al. into Myer's receiver in order to reduce costs and improve accuracy (Col. 1 lines 28-51).

Regarding claim 2, Lee et al. teaches the second divider is a programmable counter and is a divider in a system of a division to an integral multiple or a fractional-N system (Col. 2 lines 1-48 and Col. 5 line 36-Col. 6 line 6). It is well known that a divider is a programmable counter.

Regarding claim 4, Myer teaches a receiver which converts a received signal directly to a baseband signal (Col. 4 lines 55-62), comprising an oscillator 425 and 415 (Fig. 4, both the local oscillator and timing control get the same signal after the filter 405 and it gets feedback to the oscillators) generating a periodic signal; a mixer 403 (Fig. 4) for mixing the periodic signal generated by the oscillator 415 (Fig. 4, which is the same signal that gets feed into the controller 440) with the received signal, and outputting a baseband signal RBS (Fig. 4, Col. 4 lines 55-62); a switched-capacitor filter 405 (Fig. 4, Col. 5 lines 57-58) controlling a cutoff frequency when filtering the

baseband signal output from the mixer 403 (Fig. 4) according to a control signal FBC (Fig. 4) provided for a switched-capacitor element 405 (Fig. 4); and a periodic signal generated by said oscillator 415 and 425 (Fig. 4, same feedback signal) according to the received signal, characterized in that the output signal from the control signal FBC (Fig. 4) for the switched-capacitor element 405 (Fig. 4, Col. 4 line 55-Col. 5 line 58). Myer fails to teach a phase locked loop having a first and second divider used for a control signal.

Lee et al. switched capacitor bandpass filter teaches a receiver, comprising a switched-capacitor filter 334 (Fig. 5) controlling a cutoff frequency when the signal is filtered according to a control signal 1/M (Fig. 5) provided for a switched-capacitor element 334 (Fig. 5); an oscillator 326 (Fig. 5) generating a periodic signal; and a phase locked loop circuit 320 (Fig. 5) comprising a first divider 1/N (Fig. 5), wherein the PLL circuit generates a periodic signal of a predetermined frequency according to an output signal from the first divider 1/N (Fig. 5) and the periodic signal generated by the oscillator 326 (Fig. 5); and a second divider 1/M (Fig. 5) further dividing the periodic signal generated by the PLL circuit 320 (Fig. 5) according to the received signal, wherein the output signal from the second divider 1/M (Fig. 5) is provided as the control signal for the switched-capacitor element 334 (Fig. 5 and Col. 5 line 36-Col. 6 line 6).

Therefore, at the time the invention was made it would have been obvious to one skilled in the art to incorporate a divider used for a control signal as taught by Lee et al. into Myer's receiver in order to reduce costs and improve accuracy (Col. 1 lines 28-51).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Myer (US Pat# 5,012,490) in view of Lee et al. (US Pat# 5,774,555) as applied to claim 1 above, and further in view of Kultgen et al. (US Pat# 4,760,346).

Regarding claim 3, Myer's varying bandwidth digital signal detector in view of Lee et al. switched capacitor bandpass filter teaches the limitations in claim 1. Both Lee et al. and Myer fail to teach a resistor element inside the switched-capacitor filter.

Kultgen et al. switched capacitor summing amplifier teaches a switched-capacitor comprises at least an amplifier, and a resistor element R sub f (Fig. 3b), which functions as a feedback resistor of the amplifier, and is realized by the switched-capacitor element (Fig. 3b).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a resistor element inside the switched-capacitor filter as taught by Kultgen et al. into a divider used for a control signal as taught by Myer's in view of Lee et al. receiver in order to reduce costs and improve accuracy (Col. 1 lines 28-51).

Response to Arguments

Applicant's Remarks	Examiner's Response
Regarding claim 1, "Thus, Applicant respectfully submits that Lee does not disclose, teach, or suggest a second divider further dividing a periodic signal generated by a PLL circuit, wherein the	See rejection above for the new limitations.

output signal from the second divider is provided as the control signal for the switched-capacitor element and therefore even assuming, arguendo, that the teachings of Myer and Lee could have been combined by one skilled in the art as proposed by the Examiner, the invention as recited in independent claims 1 and 4 would not result."	
Regarding claim 3, "Applicant respectfully disagrees and submits that Fig. 3B merely depicts resistor R sub f, in parallel with a capacitor, in the feedback loop of an amplifier and therefore does not teach a resistor element that is realized by a switched-capacitor element."	Fig. 3b is an equivalent circuit of the summing amplifier in Fig. 2 (Col. 2 lines 31-32) which in turn is a switched capacitor (Col. 2 lines 27-28).
"The general citations provided by the Examiner do not provide the requisite teachings, suggestions or motivations to combine the teachings of Myer, Lee and Kultgen in the manner contemplated by the Examiner and therefore are insufficient	In applicant's specification page 3 lines 19-24 mentions the receiver capable of being "suitable for semiconductor integration." This is the same motivation for reducing costs (less parts, space, labor, etc....) as mentioned by the examiner.

to render claims 1-4 unpatentable over the cited references."	

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Wendell whose telephone number is 571-272-0557. The examiner can normally be reached on 7:30-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Wendell
Examiner
Art Unit 2618

9/7/2006

Quochien B. Vuong 9/12/06

QUOCHIEN B. VUONG
PRIMARY EXAMINER